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Title: Stacking Structure Of Semiconductor Chips And Semiconductor Package Using It

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Attached hereto as Exhibit A is a translation of Korean patent application 2001-12326, which was filed in Korea on March 9, 2001. I, the undersigned, certify that the document attached as Exhibit A is a true and accurate translation of Korean patent application 2001-12326.

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Dated: October 30th, 2003

[ABSTRACT]

[ABSTRACT OF DISCLOSURE]

Disclosed is a stacking structure of semiconductor chips and semiconductor package using it, capable of achieving an electric insulation even if a conductive wire makes contact with a lower surface of an upper semiconductor chip, while reducing a total thickness thereof and preventing damage. The stacking structure has a substrate formed with a plurality of circuit patterns; a first semiconductor chip bonded to an upper surface of the substrate and having a first plane and a second plane formed with a plurality of input/output pads; a spacer bonded to the second plane of the first semiconductor chip; a second semiconductor chip having first and second planes, the second plane being formed with a plurality of input/output pads, the first plane being provided with an insulating member so as to allow the second semiconductor chip to be bonded to the spacer; a first conductive wire for connecting the input/output pads of the first semiconductor chip to the circuit patterns of the substrate; and a second conductive wire for connecting the input/output pads of the second semiconductor chip to the circuit patterns of the substrate.

[REPRESENTATIVE DRAWING]

FIG. 2a

[SPECIFICATION]

[TITLE OF THE INVENTION]

STACKING STRUCTURE OF SEMICONDUCTOR CHIPS AND SEMICONDUCTOR PACKAGE USING IT

[BRIEF DESCRIPTION OF THE DRAWINGS]

FIGS. 1a and 1b are sectional views showing conventional stacking structures of semiconductor chips and semiconductor packages using the same.

FIGS. 2a to 2c are sectional views showing stacking structures of semiconductor chips according to one embodiment of the present invention.

FIG. 3 is a sectional view showing a semiconductor package according to one embodiment of the present invention.

<Reference numerals in the drawings>

11-13: stacking structures of semiconductor chips

1: first semiconductor chip	1c: input/output pad
2: second semiconductor chip	2c: input/output pad
3: spacer	4: insulating member
5: first conductive wire	6: second conductive wire
7: substrate	8: encapsulating section
9: conductive ball	14: semiconductor package

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[FIELD OF THE INVENTION AND RELATED ARTS]

The present invention relates to a stacking structure of semiconductor chips and semiconductor package using it, and more particularly to a stacking structure of

semiconductor chips and a semiconductor package using the same, capable of achieving an electric insulation even if a conductive wire makes contact with a lower surface of an upper semiconductor chip, while reducing a total thickness thereof and preventing damage.

Recently, various attempts for stacking a plurality of semiconductor chips have been made to maximize functions and performance of a semiconductor package. In order to achieve the semiconductor package, a stacking technique for the semiconductor chips is necessarily required. FIGS. 1a and 1b show a conventional stacking technique for the semiconductor chips.

As shown in FIG. 1a, a conventional stacking structure 11' includes a substrate 7', such as a printed circuit board, a circuit film, a circuit tape or a lead frame, formed at a center thereof with a first semiconductor chip 1' (edge pad type semiconductor chip). The first semiconductor chip 1' has a first plane 1a' bonded to the center of the substrate 7' by means of adhesive, and a second plane 1b' provided at a peripheral portion thereof with a plurality of input/output pads. In addition, a first plane 2a' of a second semiconductor chip 2' is bonded to a center of the second plane 1b' of the first semiconductor chip 1' by means of adhesive 4'. The second semiconductor chip 2' has a second plane 2b' formed at a peripheral portion thereof with a plurality of input/output pads 2c'. That is, the second semiconductor chip 2' is also an edge pad type semiconductor chip.

In the conventional stacking structure 11' for the semiconductor chips, a size of the second semiconductor chip 2' must be smaller than a size of the first semiconductor chip 1' in order to easily bond first conductive wires 5' to the input/output pads 1c' of the first semiconductor chip 1' and to prevent the first conductive wires 5' from making contact with each other in such a manner that a short is not created between the first conductive wires 5'.

In addition, the conventional stacking structure 11' for the semiconductor chips requires the first semiconductor chip 1' to be formed as an edge pad type semiconductor chip having a second plane formed at a center thereof with input/output pads. That is, when the first semiconductor chip 1' is a center pad type semiconductor chip having a second plane formed at a center thereof with input/output pads, it is not adaptable for the conventional stacking structure 11'. Of course, the second semiconductor chip 2' includes the center pad type semiconductor chip.

Reference numeral 6' designates a second conductive wire for connecting a circuit pattern (not shown) of the substrate 7' to the input/output pads 2c' of the second semiconductor chip 2'.

Referring to a conventional stacking structure 12' shown in FIG. 1b, it is possible to fabricate the first semiconductor chip 1' to have a size identical to or smaller than a size of the second semiconductor ship 2'. In this case, a spacer 3' having a predetermined thickness is interposed between the first plane 2a' of the semiconductor chip 2' and the second plane 1b' of the first semiconductor chip 1' in such a manner that the first conductive wire 5' bonded to the input/output pads 1c' of the first semiconductor chip 1' does not make contact with the first plane 2a' of the second semiconductor chip 2'.

Semiconductor packages including the spacer are disclosed in U.S Patent No. 5,323,060, and Japanese Patent laid-open publication Nos. 1-99248 and 5-109975.

The spacer 3' includes elastomer, urethane, vinyl, polyethylene, or acryl based adhesive tapes or films. The spacer 3' has superior adhesive, vibration-damping, impact-resistance, and heatproof characteristics so that it is mainly used in the semiconductor packaging industry.

However, the conventional stacking structure has a disadvantage that a

thickness of a semiconductor stack becomes thick because the spacer 3' having a predetermined thickness is interposed between the second plane 1b' of the first semiconductor chip 1' and the first plane 2a' of the second semiconductor chip 2'.

According to the conventional stacking structure, the thickness of the spacer 3' must be twice as compared with a loop height LH of the first conductive wire 5'. That is, as shown in FIG. 1b, a height H from an uppermost part of the first conductive wire 5' to the first plane 2a' of the second semiconductor chip 2' must be formed substantially identical to the loop height LH of the first conductive wire 5' by considering a tolerance of the loop height LH and a thickness tolerance of the spacer 3'.

In addition, when the tolerance of the loop height LH and the thickness tolerance of the spacer 3' are great, the second conductive wire 6' may be interrupted with the first plane 2a' of the second semiconductor chip 2' and a short may be created between the first conductive wires 5'.

[TECHNICAL SUBJECT MATTERS TO BE SOLVED BY THE INVENTION]

Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the prior art, and an object of the present invention is to provide a stacking structure of semiconductor chips and a semiconductor package using the same, capable of achieving an electric insulation even if a conductive wire makes contact with a lower surface of an upper semiconductor chip, while reducing a total thickness thereof and preventing damage.

[CONSTRUCTION OF THE INVENTION]

In order to accomplish the object, there is provided a stacking structure of semiconductor chips, the stacking structure comprising: a substrate formed with a

plurality of circuit patterns; a first semiconductor chip bonded to an upper surface of the substrate and having a first plane and a second plane formed with a plurality of input/output pads; a spacer bonded to the second plane of the first semiconductor chip; a second semiconductor chip having first and second planes, the second plane being formed with a plurality of input/output pads, the first plane being provided with an insulating member so as to allow the second semiconductor chip to be bonded to the spacer; a first conductive wire for connecting the input/output pads of the first semiconductor chip to the circuit patterns of the substrate; and a second conductive wire for connecting the input/output pads of the second semiconductor chip to the circuit patterns of the substrate.

The first semiconductor chip includes an edge pad type semiconductor chip, in which the input/output pads are formed at an inner peripheral portion of the second plane of the first semiconductor chip.

The spacer includes nonconductive adhesives or nonconductive adhesive tapes.

The insulating member is any one selected from the group consisting of nonconductive tapes, liquid-phase adhesives, polyimide, oxide layers, and nitride layers.

A first end of the first conductive wire is ball-bonded to the circuit patterns of the substrate and a second end of the first conductive wire is stitch-bonded to the input/output pads of the first semiconductor chip, the first end being opposite to the second end.

The input/output pads of the first semiconductor chip, to which the second end of the first conductive wire is stitch-bonded, are provided with conductive balls.

The first semiconductor chip includes a center pad type semiconductor chip, in which the input/output pads are formed at a center of the second plane of the first semiconductor chip.

The spacer includes nonconductive liquid-phase adhesives.

The insulating member is any one selected from the group consisting of nonconductive tapes, liquid-phase adhesives, polyimide, oxide layers, and nitride layers.

According to another aspect of the present invention, in order to accomplish the object, there is provided a semiconductor package comprising: a substrate formed with a plurality of circuit patterns; a first semiconductor chip bonded to an upper surface of the substrate and having a first plane and a second plane formed with a plurality of input/output pads; a spacer bonded to the second plane of the first semiconductor chip; a second semiconductor chip having first and second planes, the second plane being formed with a plurality of input/output pads, the first plane being provided with an insulating member so as to allow the second semiconductor chip to be bonded to the spacer; a first conductive wire for connecting the input/output pads of the first semiconductor chip to the circuit patterns of the substrate; a second conductive wire for connecting the input/output pads of the second semiconductor chip to the circuit patterns of the substrate; and an encapsulating section formed on the substrate in order to encapsulate the first semiconductor chip, the spacer, the second semiconductor chip having the insulating member, and the first and second wires, which are sequentially formed on one side of the substrate, by using epoxy molding compound.

The substrate is any one selected from the group consisting of a printed circuit board, a circuit tape, a circuit film and a lead frame.

When the printed circuit board, the circuit tape or the circuit film is used as the substrate, a conductive ball is welded to one side of the substrate in order to allow the substrate to be mounted on a motherboard.

According to the stacking structure of the semiconductor chips and the semiconductor package using the same, the insulating member is attached to the first

plane of the second semiconductor chip so that the stacking structure is electrically insulated even if the conductive wire makes contact with the insulating member.

Thus, the conductive wire is prevented from being damaged and the thickness of the spacer can be reduced, thereby reducing the total thickness of the stacking structure.

Furthermore, the conductive wire is fixed to the insulating layer so that the conductive wire is prevented from being biased when performing an encapsulating process.

Hereinafter, a preferred embodiment of the present invention will be described in detail with reference to accompanying drawings.

FIGS. 2a to 2c are sectional views showing stacking structures 11, 12 and 13 of semiconductor chips according to one embodiment of the present invention.

Firstly, the stacking structure 11 of the semiconductor chips shown in FIG. 2a will be described below.

As shown in FIG. 2a, the stacking structure 11 includes a substrate 7 having a substantially plate shape. The substrate 7 includes a printed circuit board, a circuit film, a circuit tape or a lead frame.

A first semiconductor chip 1 is bonded to one side of the substrate 7. The first semiconductor chip 1 has a first plane 1a and a second plane 1b formed with a plurality of input/output pads 1c.

The first semiconductor chip 1 is an edge pad type semiconductor chip, in which the input/output pads 1c are formed at an inner peripheral portion of the second plane 1b. A center pad type semiconductor chip, in which input/output pads 1c are formed at a center of the second plane 1b, will be described later with reference to FIG. 2c.

A spacer 3 having a predetermined thickness is bonded to an inner region of the second plane 1b of the first semiconductor chip 1. The spacer 3 includes nonconductive

liquid-phase adhesive or a nonconductive adhesive tape. It is possible to form the thickness of the spacer 3 identical to or less than a loop height of a first conductive wire, which will be further described later.

A second semiconductor chip 2 is provided on an upper surface of the spacer 3. The second semiconductor chip 2 has a first plane 2a and a second plane 2b. A plurality of input/output pads 2c are formed in the second plane 2b and an insulating member 4 is attached to the first plane 2a. That is, the insulating member 4 formed on the first plane 2a of the second semiconductor chip 2 is bonded to an upper portion of the spacer 3.

The insulating member 4 includes nonconductive tapes, liquid-phase adhesives, polyimide, oxide layers or nitride layers, which are widely used in a semiconductor packaging industry. In addition, the insulating member 4 is formed in a wafer before the water is divided into semiconductor chips. That is, a nonconductive tape is adhered to a rear surface of the wafer, or liquid-phase adhesive or polyimide is coated on the wafer through a printing process, a spin coating process or a spraying process. In addition, the insulating member 4 can be formed through depositing the oxide layer or nitride layer on the rear surface of the wafer.

Although the second semiconductor chip 2 is illustrated as an edge pad type semiconductor chip, in which input/output pads 2c are formed at the inner peripheral portion of the second plane 2b thereof, it is also possible to form the semiconductor chip 2 as a center pad type semiconductor chip, in which the input/output pads 2c are formed at the center of the second plane 2b of the second semiconductor chip 2.

In addition, the input/output pads 1c of the first semiconductor chip 1 are bonded to a circuit pattern of the substrate 7 through a first conductive wire 5, such as a gold wire or an aluminum wire.

In the same way, the input/output pads 2c of the second semiconductor chip 2

are bonded to the circuit pattern of the substrate 7 through a second conductive wire 6 including the gold wire and the aluminum wire.

In the stacking structure 11 of the semiconductor chips according to the present invention, the first conductive wire 5 does not directly make contact with the first plane 2a of the second semiconductor chip 2 due to the insulating member 4, so that a shorting phenomenon is not created. Thus, the first conductive wire 5 is prevented from being damaged. In addition, since the first conductive wire 5 is electrically and mechanically protected even if the first conductive wire 5 makes contact with the insulating member 4, it is possible to reduce the thickness of the spacer 3. According to the conventional stacking structure, the thickness of the spacer 3 is almost twice as compared with the loop height of the first conductive wire 5. However, according to the stacking structure of the present invention, it is possible to form the thickness of the spacer 3 identical to or smaller than the loop height of the first conductive wire 5.

Hereinafter, the stacking structure 12 of the semiconductor chips shown in FIG. 2b will be described. The stacking structure 12 shown in FIG. 2b is similar to the stacking structure 11 shown in FIG. 2a, so only the different parts of the stacking structure 12 with respect to the stacking structure 11 will be explained below.

Similar to the stacking structure 11 shown in FIG. 2a, the stacking structure 12 also includes the first semiconductor chip 1, the spacer 3, the insulating member 4, and the second semiconductor chip 2. However, the first and second conductive wires 5 and 6 are formed through a reverse bonding process instead of a normal bonding process. When forming the first and second conductive wires 5 and 6 through the normal bonding process, first ends of the conductive wires are ball-bonded to the input/output pads of the semiconductor chip and second ends of the conductive wires are stitch-bonded to the circuit pattern of the substrate. However, when forming the first and second conductive

wires 5 and 6 through the reverse bonding process, the first ends of the conductive wires are firstly ball-bonded to the circuit pattern of the substrate and the second ends of the conductive wires are stitch-bonded to the input/output pads of the semiconductor chip. Balls are formed in the input/output pads of the semiconductor chips so as to absorb impact when performing a stitch bonding process (referred to an enlarged part in FIG. 2b).

The reverse bonding process can be applicable to both first and second conductive wires 5 and 6, which connect the first and second semiconductor chips 1 and 2 to the circuit patterns of the substrate 7.

When forming the first and second conductive wires 5 and 6 through the reverse bonding process, the thickness of the spacer 3 can be further reduced. That is, since the loop height of the conductive wire, which is stitch-bonded to the input/output pads 1c, is very small, the thickness of the spacer 3 can be remarkably reduced. Alternatively, the insulating member 4 having superior adhesive force can be used as an adhesive means without using the spacer 3.

Of course, the second conductive wires 6, which connect the input/output pads 2c of the second semiconductor chip 2 to the circuit pattern of the substrate 7, can be connected to each other through a normal bonding process.

Hereinafter, the stacking structure 13 of the semiconductor chips shown in FIG. 2c will be described. The stacking structure 13 shown in FIG. 2c is similar to the stacking structure 12 shown in FIG. 2c, so only the different parts of the stacking structure 12 with respect to the stacking structure 12 will be explained below.

Similar to the stacking structure 12 shown in FIG. 2b, the stacking structure 13 also includes the first semiconductor chip 1, the spacer 3, the insulating member 4, and the second semiconductor chip 2. However, the first semiconductor chip 1 of the

stacking structure 13 is a center pad type semiconductor chip, in which a plurality of input/output pads 1c are formed at the center of the second plane 1b of the first semiconductor chip 1. In addition, input/output pads 1c of the first semiconductor chip 1 are reverse-bonded to the circuit pattern of the substrate 7 by means of the first conductive wire 5.

By using the reverse bonding technique, not only is the thickness of the spacer 3 sufficiently reduced, but also the first conductive wire 5 does not make a short with respect to a predetermined region of the first semiconductor chip 1 except for an input/output pads region while reducing the loop height of the first conductive wire 5.

Preferably, the spacer 3 includes liquid-phase adhesive. Since the second conductive wire 6 is positioned at an inner portion of the spacer 3, the liquid-phase adhesive is more efficient than a solid-type adhesive tape. That is, after reverse-bonding the input/output pads 1c of the first semiconductor chip 1 to the circuit pattern of the substrate 7 by using the first conductive wire 5, the liquid-phase adhesive is coated on the first plane 1a of the first semiconductor chip 1. Then, after the liquid-phase adhesive has been cured, the second semiconductor chip 2 having the insulating member 4 is bonded to an upper portion of the spacer 3. As described above, the insulating member 4 is any one selected from the group consisting of nonconductive tapes, liquid-phase adhesives, polyimide, oxide layers and nitride layers.

Although it is illustrated that the second semiconductor chip 2 is reverse-bonded to the substrate 7 by means of the second conductive wire 6, the second semiconductor chip 2 can be normally bonded to the substrate 7. In addition, although the second semiconductor chip 2 is illustrated as an edge type semiconductor chip, it is also possible to form the second semiconductor chip 2 as a center pad type semiconductor chip. In this case, the second conductive wire 6 is reverse-bonded to the second semiconductor

chip 2.

In addition, although the stacking structures 11, 12 and 13 are illustrated as having first and second semiconductor chips 1 and 2, third to N_{th} semiconductor chips formed at lower surfaces thereof with the insulating member 4 can be sequentially stacked on the upper surface of the second semiconductor chip 2. The number of the semiconductor chips can be varied depending on embodiments of the present invention.

FIG. 3 is a sectional view of a semiconductor package 14 having a stacking structure identical to the stacking structure 11 shown in FIG. 2a according to one embodiment of the present invention.

As shown in FIG. 3, the stacking structure of the semiconductor package 14 includes a substrate 7 formed with a plurality of circuit patterns. A first semiconductor chip 1 is bonded to one side of the substrate. The first semiconductor chip 1 has a first plane 1a and a second plane 1b formed with a plurality of input/output pads 1c.

In addition, a spacer 3 having a predetermined thickness is bonded to the second plane 1b of the first semiconductor chip 1. A second semiconductor chip is formed on an upper surface of the spacer 3. The second semiconductor chip 2 has first and second planes 2a and 2b. The second plane 2b is formed with a plurality of input/output pads 2c and the first plane 2a is formed with an insulating member in order to allow the second semiconductor chip 2 to be bonded to the spacer 3.

The input/output pads 1c of the first semiconductor chip 1 are bonded to the circuit patterns of the substrate 7 by means of first conductive wires 5 and the input/output pads 2c of the second semiconductor chip 2 are bonded to the circuit patterns of the substrate 7 by means of second conductive wires 6.

In addition, an encapsulating section 8 such as EMC (epoxy molding compound) is formed on the substrate 7 in order to encapsulate the first semiconductor chip 1, the

spacer 3, the second semiconductor chip 2 having the insulating member 4, and the first and second conductive wires 5 and 6, which are sequentially formed at one side of the substrate 7.

As described above, the substrate 7 is any one selected from the group consisting of the printed circuit board, the circuit tape, the circuit film and the lead frame. When the printed circuit board, the circuit tape or the circuit film is used as the substrate 7, a conductive ball 9 including a solder ball is welded to the circuit pattern of the substrate 7 so as to mount the substrate on a motherboard.

The stacking structures 11 and 12 shown in FIGS. 2b and 2c are applicable to the semiconductor package 14. In addition, although the semiconductor package 14 is described that it has first and second semiconductor chips 1 and 2, third to N_{th} semiconductor chips formed at lower surfaces thereof with the insulating member 4 can be sequentially stacked on the upper surface of the second semiconductor chip 2. The number of the semiconductor chips can be varied depending on embodiments of the present invention.

Although a preferred embodiment of the present invention has been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

[EFFECT OF THE INVENTION]

In the stacking structure of semiconductor chips and the semiconductor package using the same according to the present invention, the insulating member is attached to the first plane of the second semiconductor chip so that the stacking structure is electrically insulated even if the conductive wire makes contact with the insulating

member.

In addition, the insulating material is made from soft material so that the conductive wire is prevented from being damaged and the thickness of the spacer can be reduced, thereby reducing the total thickness of the stacking structure.

Furthermore, the conductive wire is fixed to the insulating layer so that the conductive wire is prevented from being biased when performing an encapsulating process.

[CLAIMS]

[Claim 1]

A stacking structure of semiconductor chips, the stacking structure comprising:

a substrate formed with a plurality of circuit patterns;

a first semiconductor chip bonded to an upper surface of the substrate and having a first plane and a second plane formed with a plurality of input/output pads;

a spacer bonded to the second plane of the first semiconductor chip;

a second semiconductor chip having first and second planes, the second plane being formed with a plurality of input/output pads, the first plane being provided with an insulating member so as to allow the second semiconductor chip to be bonded to the spacer;

a first conductive wire for connecting the input/output pads of the first semiconductor chip to the circuit patterns of the substrate; and

a second conductive wire for connecting the input/output pads of the second semiconductor chip to the circuit patterns of the substrate.

[Claim 2]

The stacking structure as claimed in claim 1, wherein the first semiconductor chip includes an edge pad type semiconductor chip, in which the input/output pads are formed at an inner peripheral portion of the second plane of the first semiconductor chip.

[Claim 3]

The stacking structure as claimed in claim 1 or 2, wherein the spacer includes nonconductive adhesives or nonconductive adhesive tapes.

[Claim 4]

The stacking structure as claimed in claim 1 or 2, wherein the insulating member is any one selected from the group consisting of nonconductive tapes, liquid-phase adhesives, polyimide, oxide layers, and nitride layers.

[Claim 5]

The stacking structure as claimed in claim 1 or 2, wherein a first end of the first conductive wire is ball-bonded to the circuit patterns of the substrate and a second end of the first conductive wire is stitch-bonded to the input/output pads of the first semiconductor chip, the first end being opposite to the second end.

[Claim 6]

The stacking structure as claimed in claim 5, wherein the input/output pads of the first semiconductor chip, to which the second end of the first conductive wire is stitch-bonded, are provided with conductive balls.

[Claim 7]

The stacking structure as claimed in claim 1, wherein the first semiconductor chip includes a center pad type semiconductor chip, in which the input/output pads are formed at a center of the second plane of the first semiconductor chip.

[Claim 8]

The stacking structure as claimed in claim 7, wherein the spacer includes nonconductive liquid-phase adhesives.

[Claim 9]

The stacking structure as claimed in claim 7, wherein the insulating member is any one selected from the group consisting of nonconductive tapes, liquid-phase adhesives, polyimide, oxide layers, and nitride layers.

[Claim 10]

A semiconductor package comprising:

a substrate formed with a plurality of circuit patterns;

a first semiconductor chip bonded to an upper surface of the substrate and having a first plane and a second plane formed with a plurality of input/output pads;

a spacer bonded to the second plane of the first semiconductor chip;

a second semiconductor chip having first and second planes, the second plane being formed with a plurality of input/output pads, the first plane being provided with an insulating member so as to allow the second semiconductor chip to be bonded to the spacer;

a first conductive wire for connecting the input/output pads of the first semiconductor chip to the circuit patterns of the substrate;

a second conductive wire for connecting the input/output pads of the second semiconductor chip to the circuit patterns of the substrate; and

an encapsulating section formed on the substrate in order to encapsulate the first semiconductor chip, the spacer, the second semiconductor chip having the insulating member, and the first and second wires, which are sequentially formed on one side of the substrate, by using epoxy molding compound.

[Claim 11]

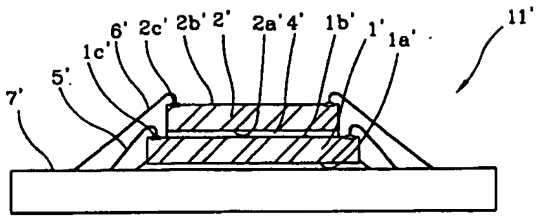
The semiconductor package as claimed in claim 10, wherein the substrate is any one selected from the group consisting of a printed circuit board, a circuit tape, a circuit film and a lead frame.

[Claim 12]

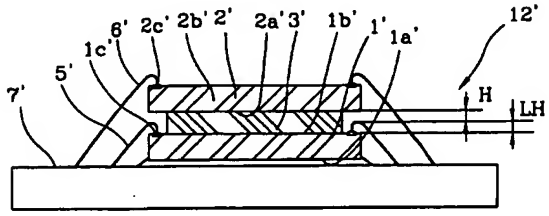
The semiconductor package as claimed in claim 10, wherein, when the printed circuit board, the circuit tape or the circuit film is used as the substrate, a conductive ball is welded to one side of the substrate in order to allow the substrate to be mounted on a motherboard.

[Figures]

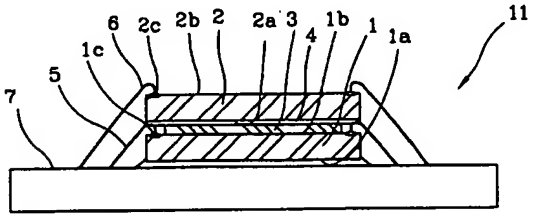
[Fig.1a]



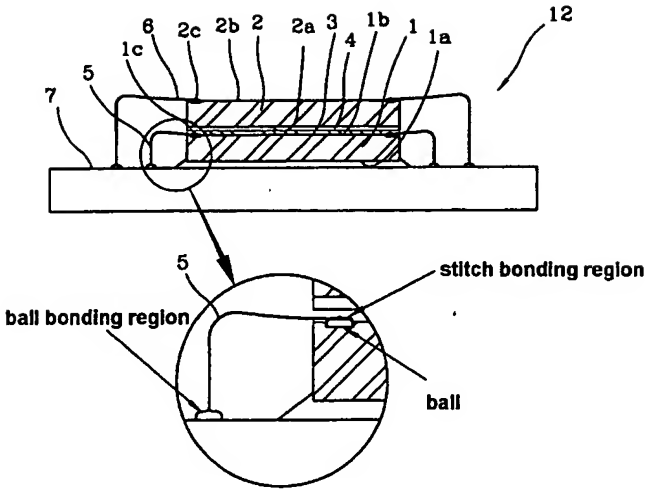
[Fig.1b]



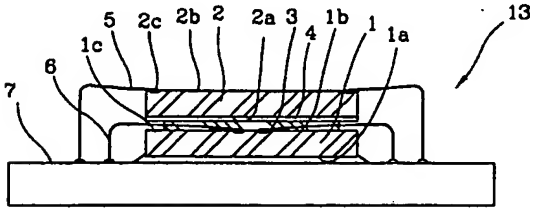
[Fig.2a]



[Fig.2b]


6
2c
2b
2
2a
3
1b
1
1a
12
1c
5
7
5
stitch bonding region
ball bonding region
ball

[Fig.2c]


5
2c
2b
2
2a
3
1b
1
1a
13
1c
6
7

[Fig.3]